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Claims

[c1] Claim 1. A Semiconductor structure formed on a substrate, comprising:
a first rigid dielectric layer;
a first non-rigid dielectric wiring level formed on the first rigid dielectric layer having at least one interconnect;
a second rigid dielectric layer formed on the first non-rigid dielectric wiring level; and
a structural securing means associated with the non-rigid dielectric wiring level for preventing a portion of the first or second rigid dielectric layers adjacent the interconnect from de-layering from the interconnect.

[c2] Claim 2. The semiconductor structure of claim 1, wherein the structural securing means comprises at least one dummy fill shape in proximity to the interconnect having a coefficient of thermal expansion better matched to the first and second rigid dielectric layer than that of the non-rigid dielectric wiring level.

[c3] Claim 3. The semiconductor structure of claim 2, wherein the at least one dummy fill shape is one of an alloy predominately composed of copper, aluminum and tungsten.

[c4] Claim 4. The semiconductor structure of claim 2, wherein an effective CTE of a region of the first non-rigid dielectric wiring level is reduced in proportion to a density of the at least one dummy metal fill shape.

[c5] Claim 5. The semiconductor structure of claim 1, wherein the structural securing means are a plurality of dummy fill shapes aligned in rows and columns about the interconnect.

[c6] Claim 6. The semiconductor structure of claim 1, wherein the structural securing means is matched to an overall average local metal density such that CTE mis-match stresses and deflections are substantially toward zero.

[c7] Claim 7. The semiconductor structure of claim 1, wherein the structural securing means reduces tempera-ture-driven stress.

[c8] Claim 8. The semiconductor structure of claim 1, wherein the structural securing means inhibits deflecting of the first and second rigid dielectric layer.

[c9] Claim 9. The semiconductor structure of claim 1, wherein:
the interconnect has a line width from .1 microns to

greater than 1 micron;
the structural securing means are dummy fill shapes adjacent to the interconnect;
the dummy fill shapes are one of an alloy substantially composed of aluminum, copper and tungsten; and
the dummy metal fill shapes are electrically isolated from each other and the interconnect.

[c10] Claim 10. The semiconductor structure of claim 9, wherein a minimum spacing between the dummy fill shapes are one to four times a maximum spacing for a level.

[c11] Claim 11. The semiconductor structure of claim 9, wherein a minimum spacing between the dummy fill shapes are equal to a minimum spacing width for a level.

[c12] Claim 12. The semiconductor structure of claim 9, wherein a density of the dummy fill shapes is between approximately 45% and 50%.

[c13] Claim 13. The semiconductor structure of claim 9, wherein a width and length of the dummy fill shapes are 3x a minimum line width of the interconnect.

[c14] Claim 14. The semiconductor structure of claim 1, wherein the structural securing means are dummy fill shapes arranged in a staggered offset pattern surround-

ing the interconnect.

[c15] Claim 15. The semiconductor structure of claim 1, wherein the first non-rigid dielectric wiring level is a low-k dielectric siloxane based semi-organic layer.

[c16] Claim 16. The semiconductor structure of claim 15, wherein the first and second rigid dielectric layer contains silicon oxide based glass.

[c17] Claim 17. The semiconductor structure of claim 1, wherein the structural securing means are a plurality of square shaped dummy fill shapes arranged in a staggered pattern in the first non-rigid dielectric wiring level.

[c18] Claim 18. A semiconductor structure, comprising:
a first rigid dielectric layer;
a second rigid dielectric layer;
a first non-rigid low-k dielectric layer formed between the first and second rigid dielectric layer; and
a plurality of dummy fill shapes formed in the first non-rigid layer which replace portions of the first non-rigid low-k dielectric layer with lower coefficient of thermal expansion (CTE) metal such that an overall CTE of the first non-rigid low-k dielectric layer and the plurality of dummy fill shapes matches a CTE of the first and second rigid dielectric layers more closely than that of the first

non-rigid low-k dielectric layer alone.

[c19] Claim 19. The semiconductor structure of claim 18, wherein the first and second dielectric layer and the first non-rigid layer have stresses and deflections which tends toward zero.

[c20] Claim 20. The semiconductor structure of claim 18, wherein the plurality of dummy metal fill shapes reduce temperature-driven stress between the first and second rigid dielectric layer and the first non-rigid low-k dielectric layer.

[c21] Claim 21. The semiconductor structure of claim 18, further comprising a substrate and at least one front-end-of-line (FEOL) device formed on the substrate, the first rigid dielectric layer is formed on the FEOL.

[c22] Claim 22. The semiconductor structure of claim 18, wherein the plurality of dummy metal fill shapes are substantially composed of one of an alloy of copper, tungsten and aluminum and extend between a bottom surface of the second rigid dielectric layer and top surface of the first rigid dielectric layer, and the first and second rigid dielectric layer comprise a silicon oxide based glass.

[c23] Claim 23. The semiconductor structure of claim 18,

further comprising:

a second non-rigid low-k dielectric layer formed on the second rigid dielectric layer;

a third rigid dielectric layer formed on the second non-rigid low-k dielectric layer;

a metal interconnect extending between the second and third rigid dielectric layer and formed in the second non-rigid low-k dielectric layer; and

at least one dummy fill shape formed in the second non-rigid low-k dielectric layer in proximity to the metal interconnect, the at least one dummy fill shape being formed of a material such that an overall CTE of the at least one dummy fill shape better matches to the second and third rigid dielectric layer than that of the second non-rigid low-k dielectric layer.

[c24] Claim 24. A structure, comprising:

a substrate;

at least one front-end-of-line (FEOL) device formed on the substrate;

a first rigid layer comprising a dielectric formed on the at least one FEOL device;

a first non-rigid layer comprising a low-k dielectric siloxane based semi-organic layer formed on first rigid layer;

a second rigid layer comprising a dielectric formed on

the first non-rigid layer;
a second non-rigid layer comprising a low-k dielectric formed on second rigid layer;
a third rigid layer formed on the second non-rigid layer;
at least one interconnect formed in the second non-rigid layer extending between the second and third rigid layer; and
at least one dummy fill shape formed in the second non-rigid layer extending between the second and third rigid layer, the at least one dummy fill shape being positioned in a susceptible area in proximity to the interconnect to maximize strength to the structure and prevent the second and third rigid layer adjacent the interconnect from de-layering away from the interconnect.

[c25] Claim 25. The structure of claim 24, wherein:
the at least one dummy fill shape is a plurality of dummy fill shapes made of one of an alloy substantially composed of aluminum, copper and tungsten;
a minimum spacing between each of the plurality of dummy fill shapes are substantially equal to a minimum line width for a level forming a density of approximately between 45% and 50%; and
the first, second and third rigid layers are composed of silicon oxide.

[c26] Claim 26. The semiconductor structure of claim 25, wherein the plurality of dummy fill shapes are arranged in a staggered pattern in the second non-rigid layer.

[c27] Claim 27. The semiconductor structure of claim 24, wherein the at least one dummy fill shape is substantially square.

[c28] Claim 28. The semiconductor structure of claim 24, wherein the at least one dummy fill shape are several dummy fill shapes aligned in rows and columns in the second non-rigid layer.

[c29] Claim 29. The semiconductor structure of claim 24, wherein the dummy fill shapes are composed of an alloy having a coefficient of thermal expansion (CTE) which better matches to a CTE of the second and third rigid layer such than the first non-rigid layer.

[c30] Claim 30. A process of forming a semiconductor structure, comprising:
forming a first rigid dielectric layer;
forming a first non-rigid dielectric wiring level on the first rigid dielectric layer having an interconnect;
forming a second rigid dielectric layer on the first non-rigid dielectric wiring level; and
forming a plurality of dummy metal fill shapes in the first

non-rigid dielectric wiring level in proximity to the interconnect for preventing a portion of the first or second rigid dielectric layers adjacent the interconnect from de-layering away from the interconnect.

[c31] Claim 31. The process of claim 30, wherein the forming of the plurality of dummy fill shapes includes forming a density of approximately 45% to 50%.